Optical Communication DSP Equalization

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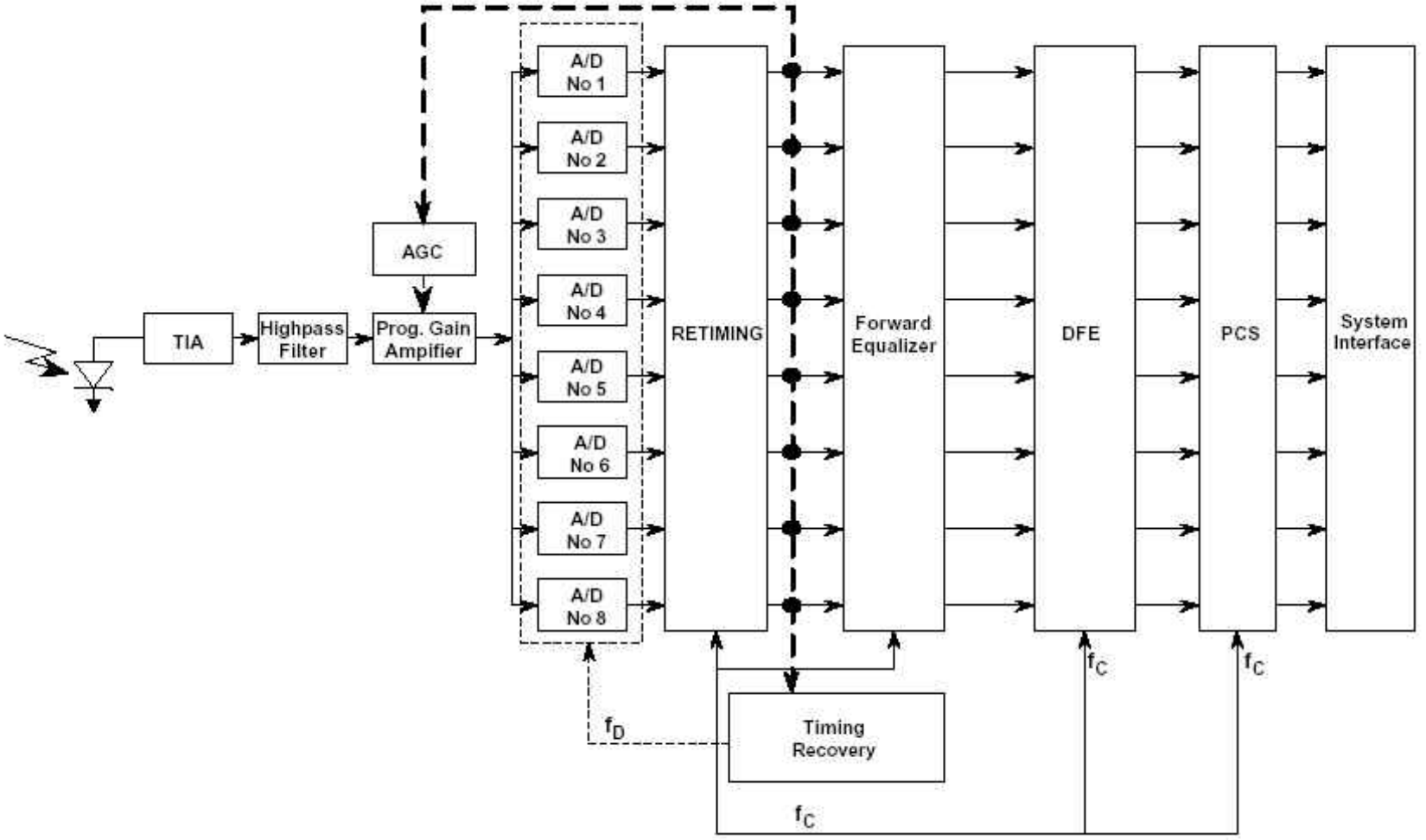
Main Implementation Challenge

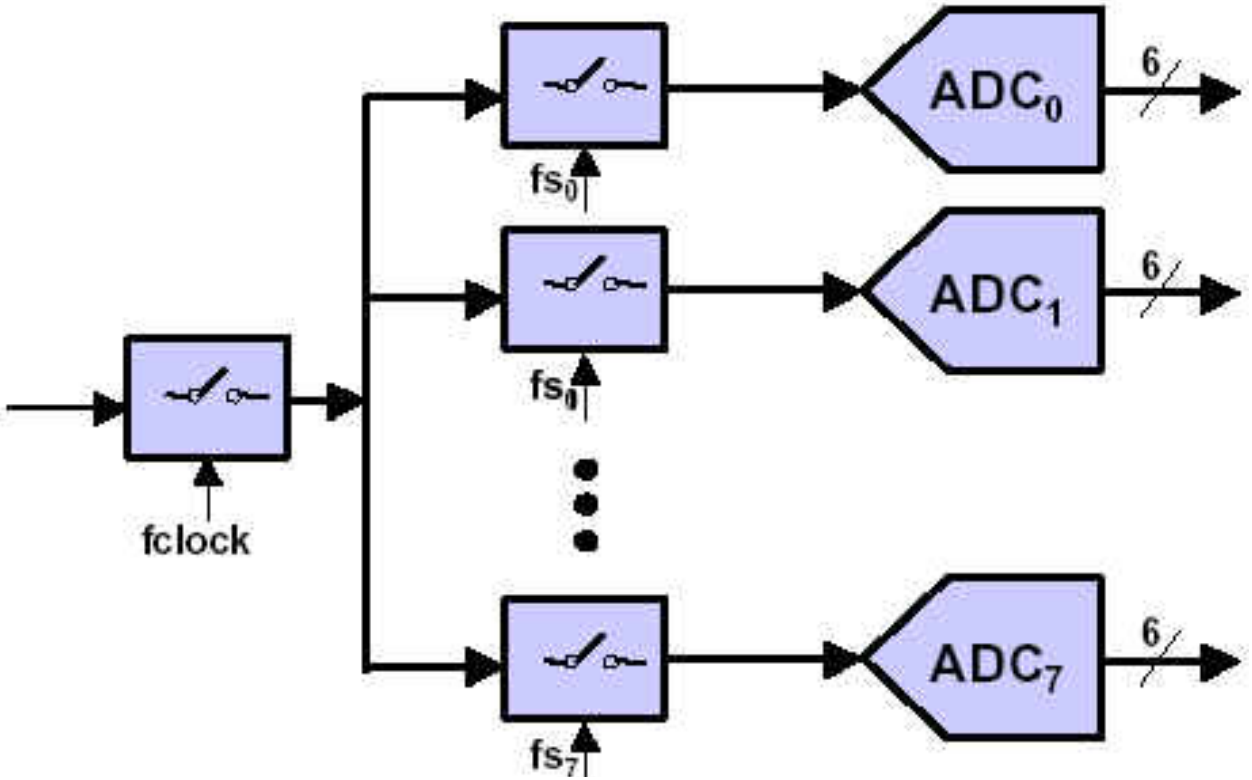
- How to implement A/D conversion & DSP function for multi-gigabit rates(3.125G for 10GBase-LX4).
- One solution is “Parallel Processing (Block Processing)”.

Block Processing DSP Architecture [1]



Interleaved ADC [2][3]

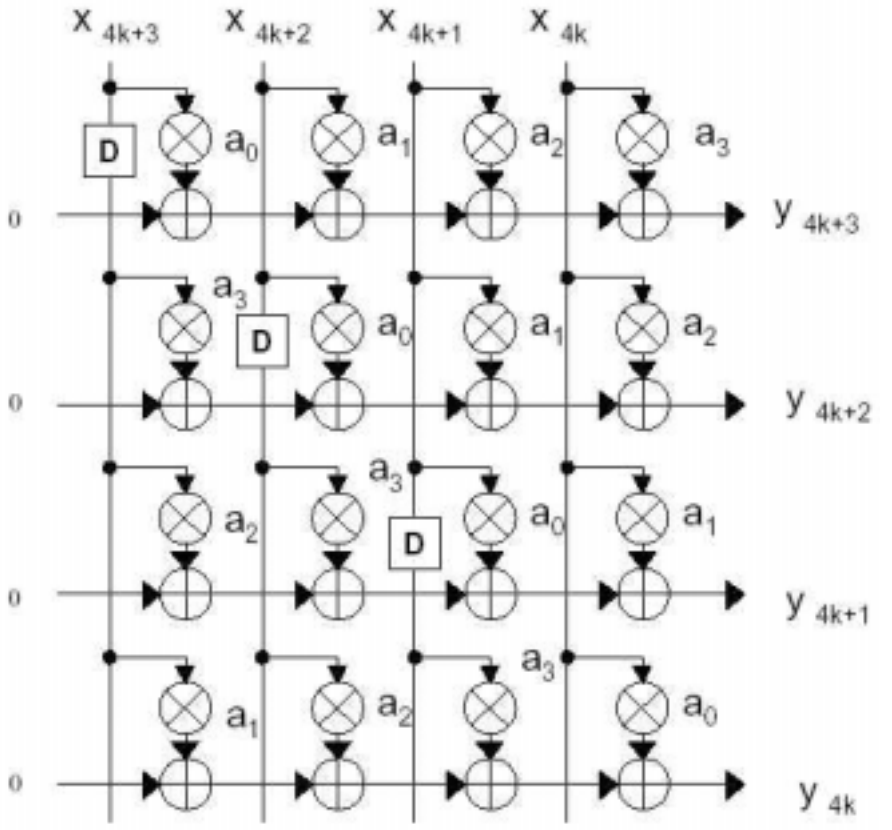
- Difficulty in the deign of an up-front interleaved T/H. (100-ps spacing for 10-GS/s, i.e. 320-ps spacing for 3.125GS/s).



Feedforward Equalization

4-Parallel 4-Tap FIR Filter

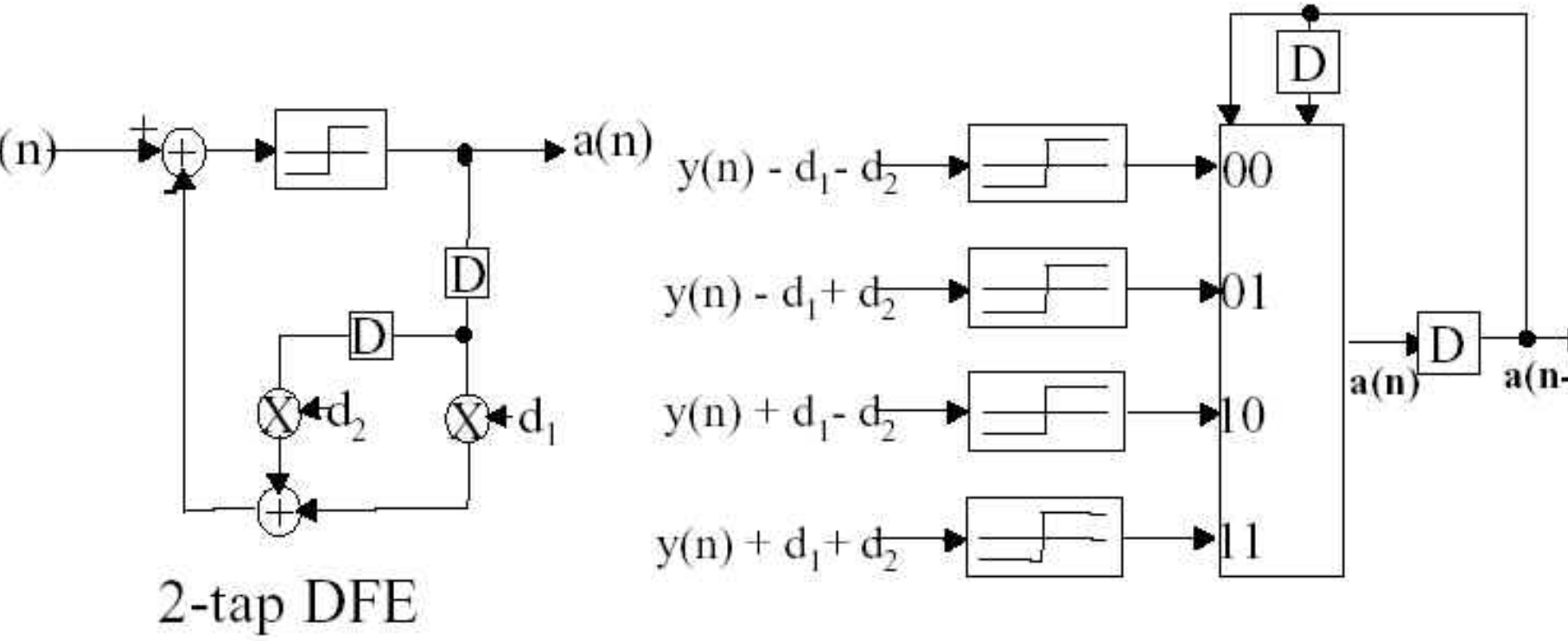
- Parallel FFE (straightforward).



$$y(n) = a_0\,x(n) + a_1\,x(n-1) + a_2\,x(n-2) + a_3\,x(n-3)$$

DFE Loop Reformulation

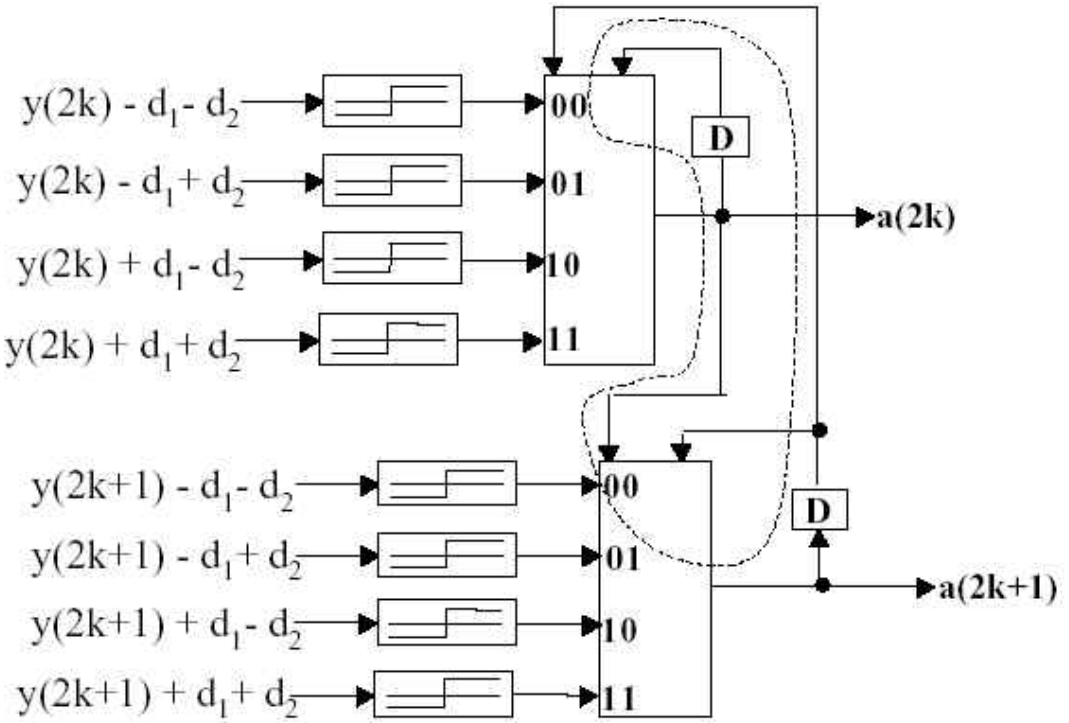
- Complexity grows as K^N for a N-tap DFE (K-level modulation).
- Speed limited by a 2-to-1 MUX (0.2ns in 0.13 μ m [2]).



L-parallel

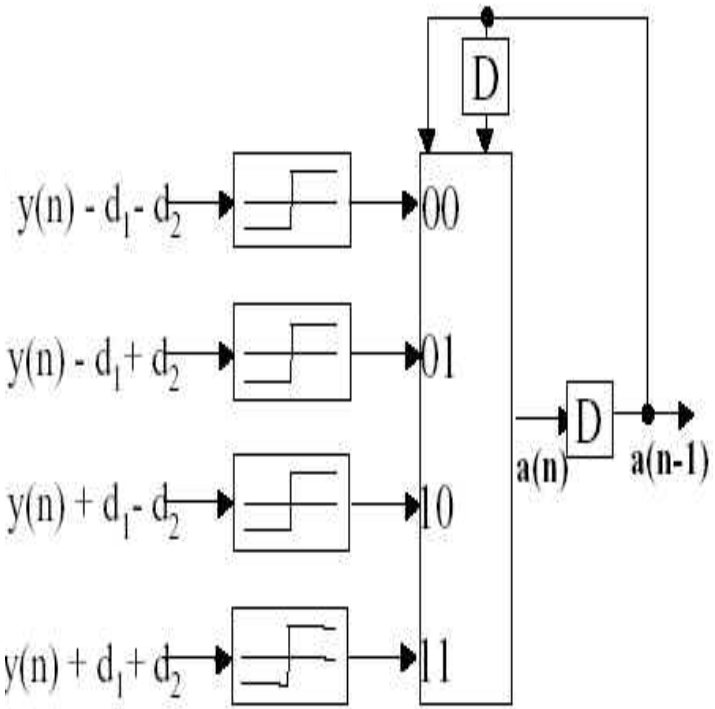
- Complexity ~L*K^N for L-parallel and N-tap DFE (K-level modulation).
- Speed limited by a L MUX. (L< 5 for 1 GHz clock).

2-Parallel Implementation



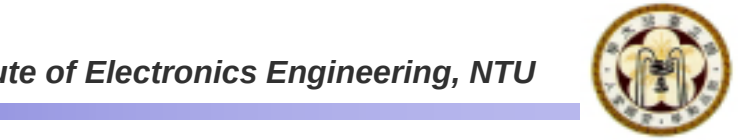
Look-ahead (con't)

- Eliminate dependency between a(n) and a(n-1)



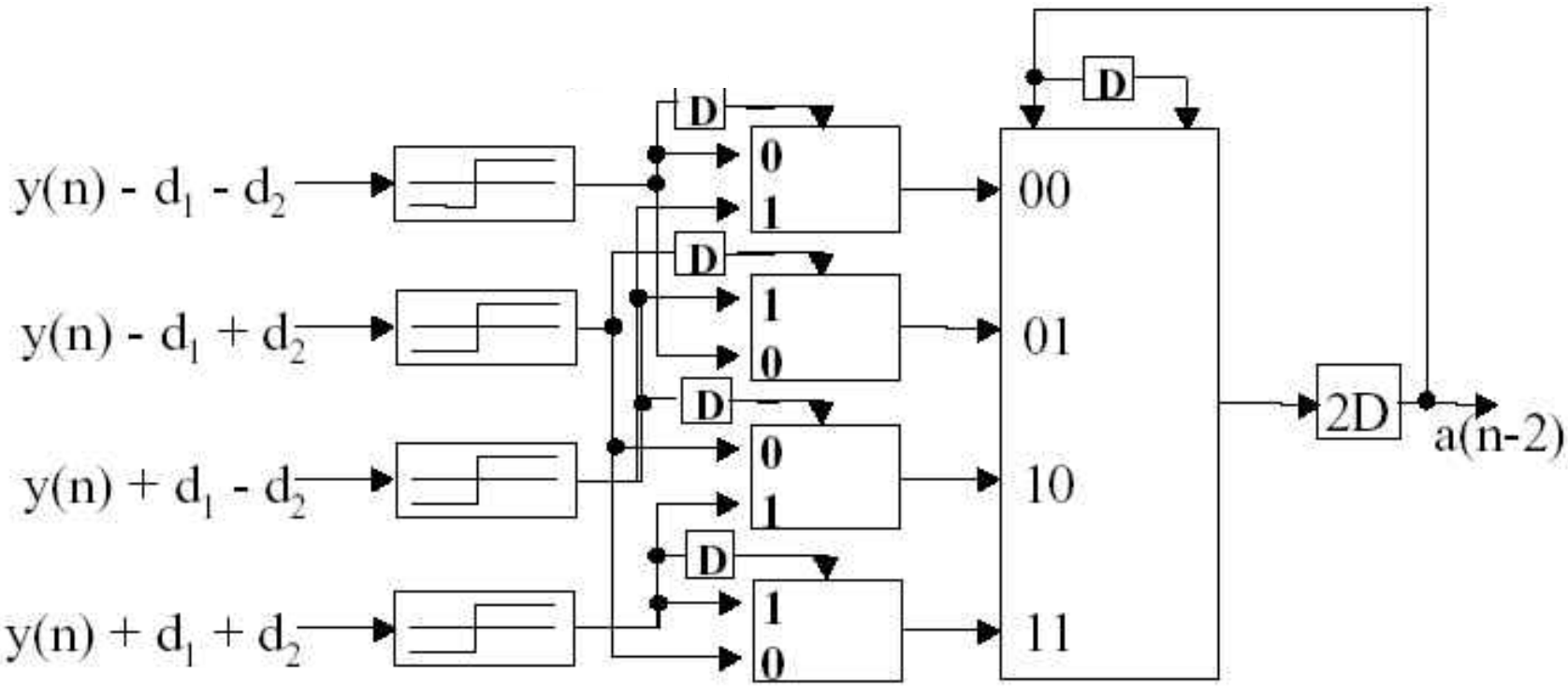
$$a(n) = f_1(n)\bar{a}(n-1)\bar{a}(n-2) + f_2(n)\bar{a}(n-1)a(n-2) + f_3(n)a(n-1)\bar{a}(n-2) + f_4(n)a(n-1)a(n-2)$$

$$= [f_1(n)\bar{f}_1(n-1) + f_3(n)f_1(n-1)]\,\bar{a}(n-2)\bar{a}(n-3) + [f_1(n)\bar{f}_2(n-1) + f_3(n)f_2(n-1)]\,\bar{a}(n-2)a(n-3) + [f_2(n)\bar{f}_3(n-1) + f_4(n)f_3(n-1)]\,a(n-2)\bar{a}(n-3) + [f_2(n)\bar{f}_4(n-1) + f_4(n)f_4(n-1)]\,a(n-2)a(n-3)$$



Look-ahead (con't)

- Extra register can use to pipeline the critical path.



Parameter comparison

	[1]	[2]
ADC wordlength	5-bit	6-bit
FFE tap number	5	8
DFE tap number	3	6

Area and Power Estimates [2]

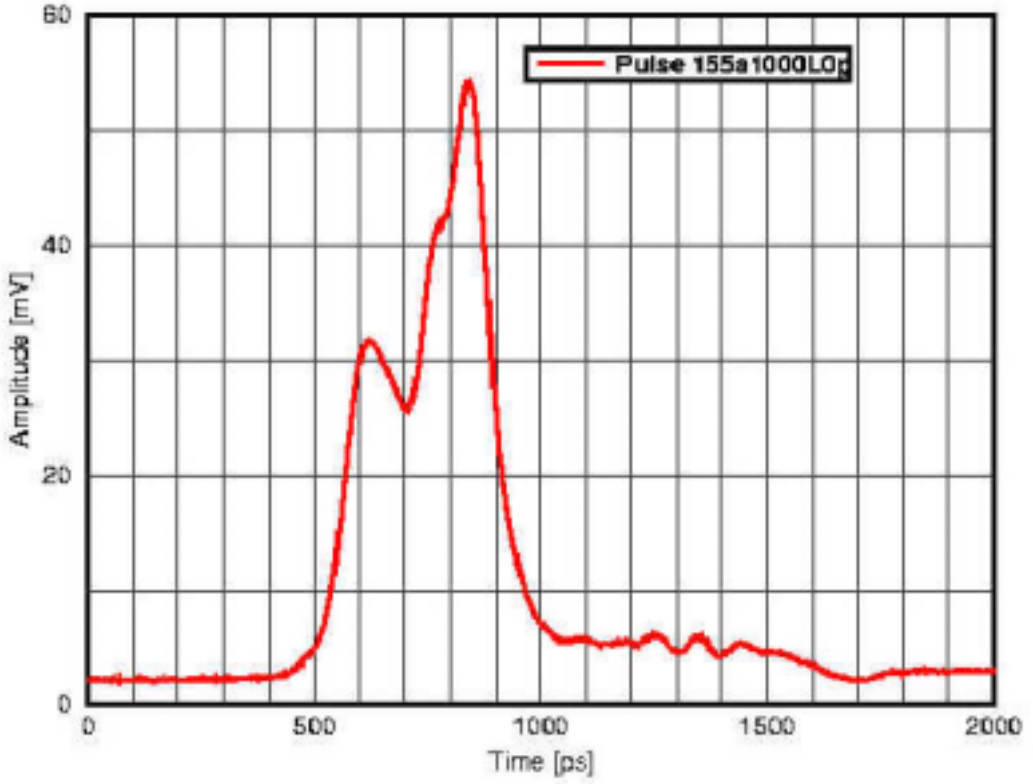
- Assumed technology: Digital 0.13 µm CMOS, Analog 0.18 µm SiGe.
- FFE 8-tap, DFE 6-tap.
- DSP parallelization factor 8 (1.25 GHz clock speed).
- ADC parallelization factor 8.

Component	Area	Power
Analog	----	0.45Watts
DSP	1mm^2	0.8Watts
Total	----	~1.25Watts

Experiment Result (con't) [2]

Fiber Impulse Response

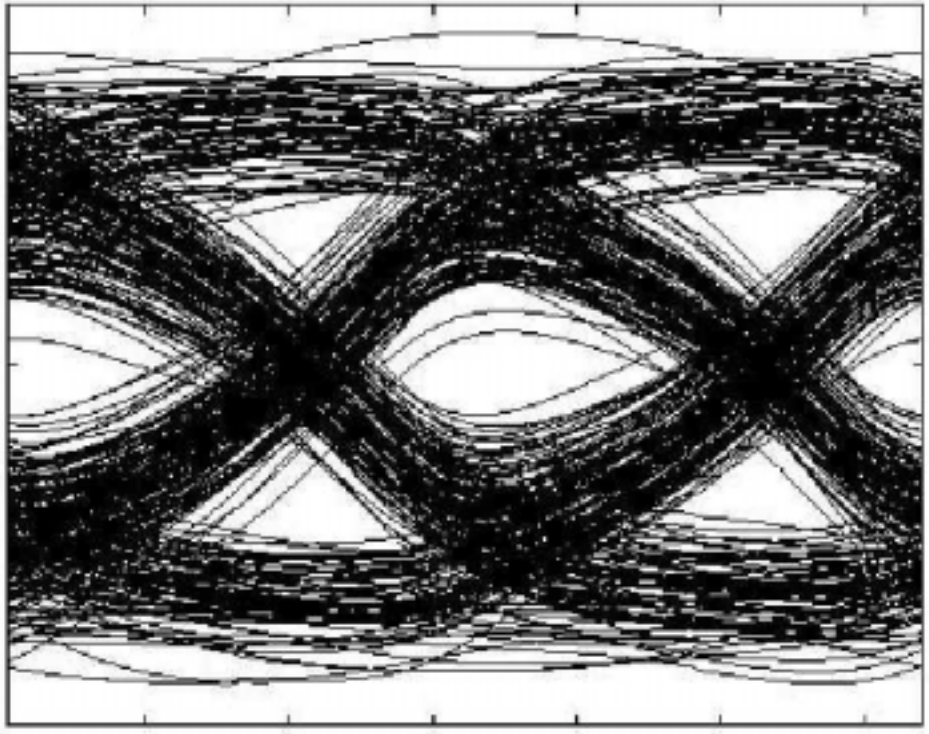
(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Experiment Result (con't) [2]

Eye Pattern at Input of A/D (3.125Gb/s)

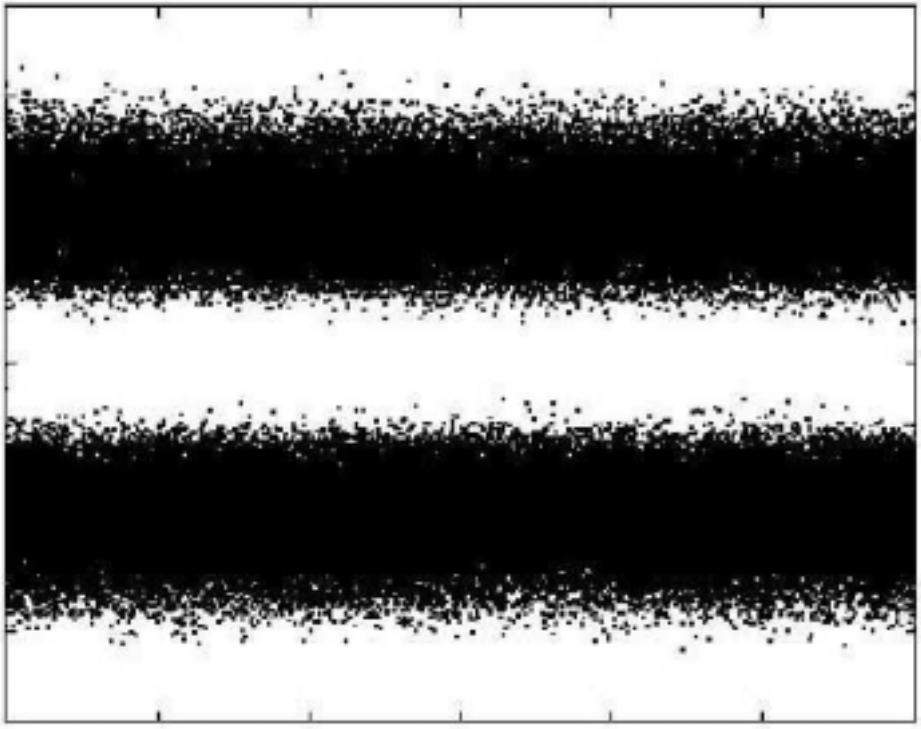
(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Experiment Result (con't) [2]

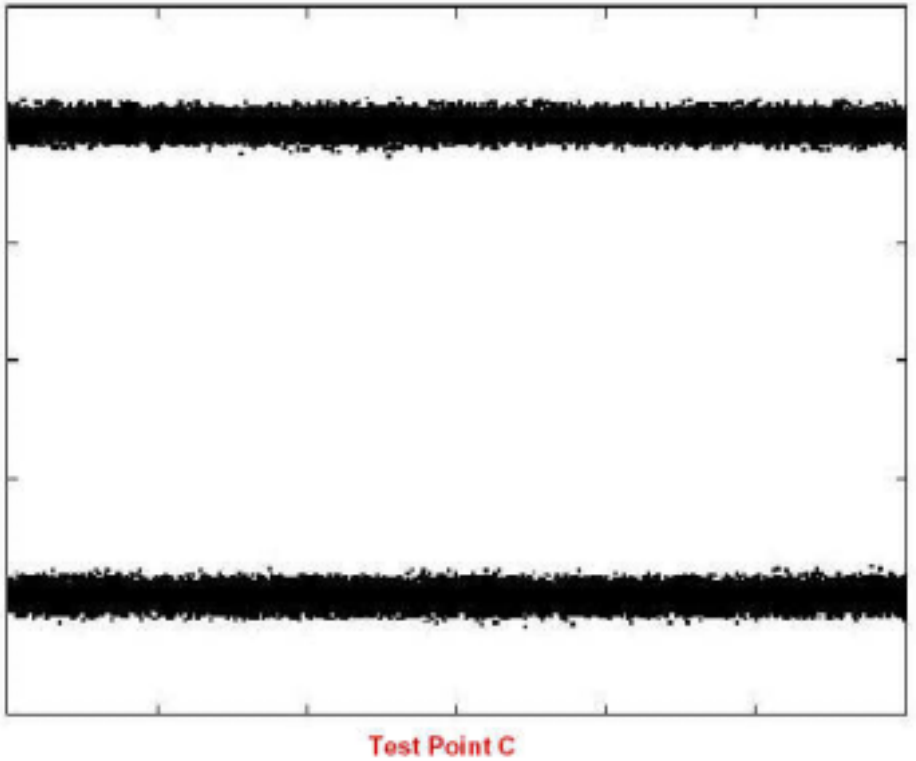
Eye Pattern at Output of A/D (3.125Gb/s)

(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Experiment Result (con't) [2]

Equalized Eye Pattern at Input of Slicer (3.125Gb/s)
(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



SNR = 28dB

Future Work

- Determine the EQ parameters
  - FFE tap numbers
  - DFE tap numbers
- Low-power, Low-cost implementation.

Reference

[1],K. Azadet *et al.*, “Equalization and FEC Techniques for Optical Transceivers,” in IEEE Journal of Solid-State Circuits, vol. 37, no. 3, March 2002.

[2],O. Agazzi *et al.*, “DSP-Based Equalization for Optical Channels,” IEEE 802.3ae meeting, New Orleans, September 12-14, 2000.

[3],K. Poulton et al. , “A 4GSample/s 8b ADC in 0.35um CMOS,” ISSCC 2002/Session 10/High-speed ADCs/10.1

[4],K. Azadet and Meng-Lin Yu, “An Arbitrarily Fast Block Processing Architecture for Decision Feedback Equalizers,” in *Proc. VLSI Technology Systems and Applications Conf.*,1999, pp. 175-178.